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09/742,383	12/22/2000	Moo Jin Lee	2658-0251P	9446

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EXAMINER
DHARIA, PRABODH M

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/742,383	Applicant(s) LEE, MOO JIN	
	Examiner Prabodh M Dharia	Art Unit 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

3. The abstract of the disclosure is objected to because number of words exceed 150.

Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3,6-10,12,14,15-19,22,23,25,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937).

Regarding Claim 1, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21) including a plurality of liquid crystal cells arranged at each intersection between data lines and gate lines (Scan Line) (figure 6, Col. 6, Lines 20-25) to control a light transmissivity in response to data signals from the data lines, (Col. 9, Line 57 to Col. 10, Line 4) and a plurality of switching devices for switching the data signals to be applied from the data lines to the liquid crystal cells (Col. 9, Lines 36-41) in response to signals on the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

However, Katakura fails to teach Scan Lines, which are connected to the Gate Lines to drive LCD display.

However, it is well known to one in the ordinary skill in the art that in an active matrix type LCD the scan lines are connected to the gate lines and video information is connected to drain of the pixel driving transistor. The reference cited of Kikuo et al. also teaches gate lines

and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Kikuo et al. teaching in Katakura et al. teaching to have a high luminance output, accurate gray levels, minimizes display artifacts and flickering.

Regarding Claim 2, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 3, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 6, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36) for a liquid crystal display panel (101, figure 8, Col. 9, Lines

20,21) including a plurality of liquid crystal cells arranged at each intersection between data lines and gate lines (Scan Line) (figure 6, Col. 6, Lines 20-25) to control a light transmissivity in response to data signals from the data lines, (Col. 9, Line 57 to Col. 10, Line 4) and a plurality of switching devices for switching the data signals to be applied from the data lines to the liquid crystal cells (Col. 9, Lines 36-41) in response to signals on the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

it is well kown to one in the ordinary skill in the art that in an active matrix type LCD the scan lines are connected to the gate lines and video information is connected to drain of the pixel driving transistor. The reference cited of Kikuo et al. also teaches gate lines and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49).

Regarding Claim 7, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line

driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 8, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61).

Regarding Claim 9, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21); a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30). Kikuo et al. also teaches gate lines and gate line driver are connected to scan line and scan line driver respectively (Col. 20, Lines 23-25, Col. 22, Lines 26,27, Col. 18, Lines 44-49); a voltage converter generating a high level gate voltage (Col. 15, Lines 55-60); a gate line controller receiving the high level gate voltage from the voltage converter (Col. 17, Lines 23-26) and supplying a controlling signal that varies as an ambient temperature varies (Col. 8, Lines 8-11, Col. 29, Lines 43-62); and a gate line driver receiving the controlling signal from the gate line controller and driving a gate line (Col. 29, Lines 43-64, Col. 32, Lines 9-20).

Regarding Claim 10, Katakura et al. teaches the gate line (Scan Line) controller is a current controller such that the controlling signal received by the gate line (Scan Line) driver includes an electrical current, an amount of which varies as the ambient temperature varies (Col. 5, Lines 31-40).

Regarding Claim 12, Kikuo et al. teaches the current controller includes a thermistor (Col. 17, Lines 28-30, Col. 29, Lines 50-60).

Regarding Claim 14, Kikuo et al. teaches the current controller (Col. 17, Lines 28-30, Col. 29, Lines 50-60), further includes a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 15, Kikuo et al. teaches gate line controller is a voltage divider such that the controlling Signal received by the gate line driver includes a voltage, a level of which varies as the ambient temperature varies (Col. 16, Lines 39-47, Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 16, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61); the voltage divider decreases the voltage as the ambient temperature increases (Col. 29, Lines 42-62).

Regarding Claim 17, Kikuo et al. teaches the current controller includes a thermistor (Col. 17, Lines 28-30, Col. 29, Lines 50-60).

Regarding Claim 18, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61).

Regarding Claim 19, Kikuo et al. teaches the voltage divider (Col. 13, Lines 61-65) further includes a resistor (Col. 13, Lines 61-65)such that the resistor is connect-between the voltage converter (Col. 13, Lines 37,38) and an input to the gate line driver (Col. 16, Lines 39-47, Col. 29, Lines 42-62, Col. 32, Lines 9-20) and the negative temperature coefficient thermistor (Col. 13, Lines 56-58) is connected between ground (reference voltage) (figure27, Col. 29, Lines 42-55) and the input to the gate line driver (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

Regarding Claim 22, Katakura et al. teaches a charge characteristic compensating circuit (106, figure 8, Col. 9, Lines 33-36) for a liquid crystal display panel (101, figure 8, Col. 9, Lines 20,21); comprising: a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from

the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

Kikuo et al. teaches a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

Regarding Claim 23, Katakura et al. teaches the gate line (Scan Line) controller is a current controller such that the controlling signal received by the gate line (Scan Line) driver includes an electrical current, an amount of which varies as the ambient temperature varies (Col. 5, Lines 31-40).

Regarding Claim 25, Katakura et al. teaches the gate lines (Scan Lines), the circuit comprising (Col. 6, Lines 8-10): a voltage supply for generating a gate voltage required for the gate lines (Scan Lines) (figure 3, Col. 5, Lines 25-29); a gate line driver for applying the gate voltage from the voltage supply to the gate lines to drive the gate lines (figure 3, Col. 5, Lines 25-29); and a current controller for responding to a change in the ambient temperature to change an amount of current (Col. 5, Lines 31-40) of the gate voltage to be applied from the voltage supply to the gate line driver (Col. 5, Lines 27-30).

Regarding Claim 26, Kikuo et al. teaches the thermistor is a negative temperature coefficient thermistor (Col. 13, Lines 56-61); the voltage divider decreases the voltage as the ambient temperature increases (Col. 29, Lines 42-62).

6. Claims 4,11,13,24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937) as applied to claims 1-3,6-10,12,14,15-19,22,23,25,26 above, and further in view of Marks et al. (5,119,215).

Regarding Claim 4, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

However, Katakura et al. modified by Kikuo fails to teach the thermistor is a positive temperature coefficient thermistor.

However, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Marls et al. teaching in Katakura et al. modified by Kikuo et al. teaching to have a high luminance output, and minimizes display artifacts.

Regarding Claim 5, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Regarding Claim 11, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52). It is well known to one in the ordinary skill in the art that the positive temperature coefficient thermistor increases impedence with the increase in temperature and with the voltage applied the current controller decreases the amount of current as the ambient temperature increases.

Regarding Claim 13, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52).

Regarding Claim 24, Marks et al. teaches the thermistor is a positive temperature coefficient thermistor (Col. 4, Lines 49-52). It is well known to one in the ordinary skill in the art that the positive temperature coefficient thermistor increases impedence with the increase in temperature and with the voltage applied the current controller decreases the amount of current as the ambient temperature increases.

7. Claims 20, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katakura et al. (5,754,154) in view of Kikuo et al. (5,250,937) as applied to claims 1-3,6-10,12,14,15-19,22,23,25,26 above, and further in view of Noma et al. (6,184,631 B1).

Regarding Claim 20, Katakura et al. teaches the current controller (Col. 9, Lines 20-44) and correction circuit is connected between the voltage supply and the gate line driver (Col. 5, Lines 27-40). Kikuo et al. teaches a resistor and a thermistor connected, in parallel (Col. 13 Lines 42-50), between the voltage supply connected to the correction circuit and also the gate line driver by using the corrected voltage super imposed on the clock CL1 that generates horizontal scan lines and vertical scan lines driving gate lines (Col. 29, Lines 42-62, Col. 32, Lines 9-20).

However, Katakura et al. modified by Kikuo fails to teach the voltage divider further includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver.

However, Noma et al. teaches the voltage divider further includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver (Col. 12, Lines 65-67, Col. 10, Lines 58-60) and Kikuo et al. teaches the negative temperature coefficient thermistor (Col. 13, Lines 56-58) is connected between ground (reference voltage) (figure27, Col. 29, Lines 42-55) and the input to the gate line driver (Col. 29, Lines 42-62, Col. 32, Lines 9-20) .

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate Noma et al. teaching in Katakura et al. modified by Kikuo et al. teaching to have a high luminance output, accurate gray levels, minimizes display artifacts and flickering by supplying constant liquid current to LCD display.

Regarding Claim 21, Noma et al. teaches teaches the voltage divider includes a positive temperature coefficient thermistor such that the positive temperature coefficient thermistor is connected between the voltage converter and an input to the gate line driver and a resistor such that the resistor is connected between ground and the input to the gate line driver (Col. 12, Line 62 to Col. 13 Line 6, Col. 10, Lines 58-60)

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is informed that all of the other additional cited references render the claims obvious.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Odaohhara (6,396,243 B2) Power unit aqnd power source switching apparatus for a computer.

Iwasaki et al. (6,075,511) Drive voltages switched depending upon temperature detection of chiral smectic liquid crystal display.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M Dharia whose telephone number is 703-605-1231. The examiner can normally be reached on M-F 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-3054938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9341 for regular communications and 703-872-9341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

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March 4, 2003

Amare Mengistu
Primary Examiner